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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/658,781	09/10/2003	Yasuhisa Ishikawa	02410342AA	3907

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EXAMINER	
LEE, EUGENE	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/08/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/658,781	ISHIKAWA ET AL.	
	Examiner	Art Unit	
	Eugene Lee	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 December 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: element 41, 49, and 50 (see, for example, FIG. 4). Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

2. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the field effect transistors share a gate (claim 4) must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet,

even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

4. Claim 6 is objected to because of the following informalities: the word "diffused" is misspelled. Appropriate correction is required.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claim 4 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specification does not describe how field effect transistors can share a gate and still be considered separate field effect transistors.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1 thru 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In line 9 of claim 1, it is not clear what the applicant is referring to in the limitation "its periphery" and whether the periphery is referring back to "a diffused region", "well region", or "substrate." For the sake of compact prosecution, the Examiner is interpreting the limitation to mean any region outside "a diffused region", however, proper clarification and correction are required.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1, and 6 are rejected under 35 U.S.C. 102(e) as being anticipated by Ker et al. 6,573,566 B2. Ker discloses (see, for example, FIG. 6A) a SOI-SCR device (semiconductor device) comprising a silicon layer (substrate), P-well (well region) 136, field effect transistor, second first-type doped region (diffused region) 154, and a PN junction. In FIG. 6B, Ker discloses the second first-type doped region 154 across the P-well 136 and silicon layer. A voltage potential may be applied to the second first-type doped region to affect the potential in the P-well. A PN junction is formed between the second first-type doped region 154 and a third second-type doped region (periphery) 152. In FIG. 6A, (+) and (-) terminals are shown. In FIG. 9C, the SOI-SCR device is connected to an internal circuit and in column 11, lines 24-27, Ker states ESD current is channeled away without entering the internal circuit.

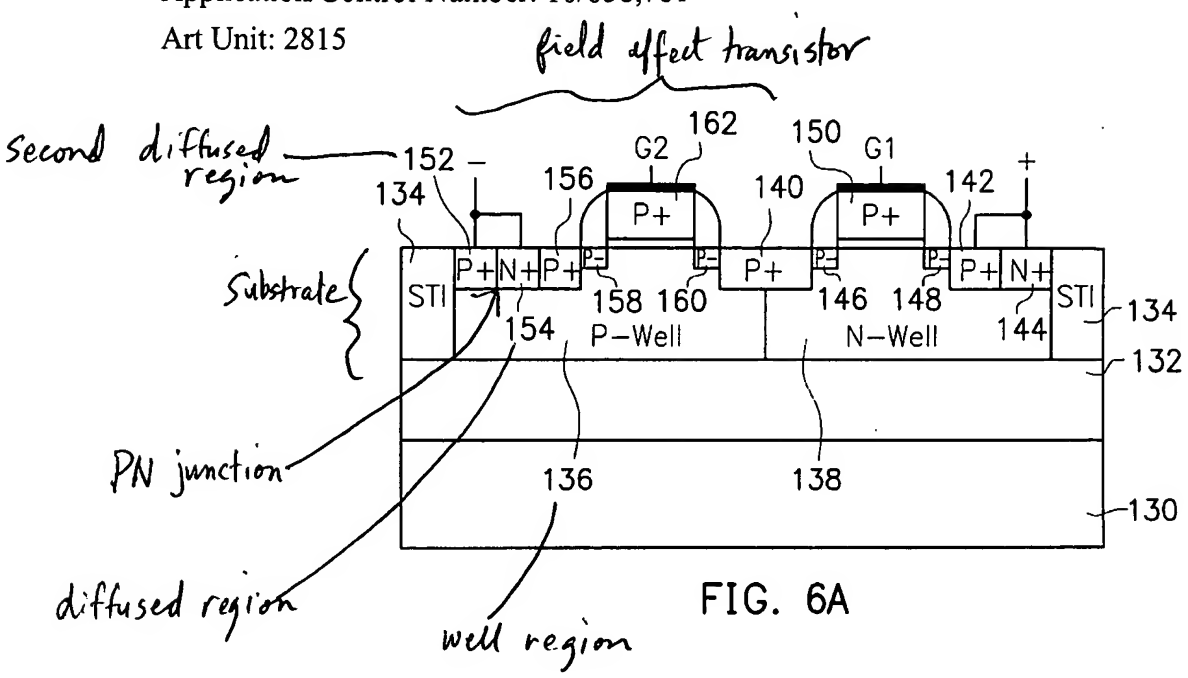

FIG. 6A

Regarding claim 6, see, for example, a third second-type doped region (second diffused region) 152.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. '566 B2 as applied to claims 1 and 6 above, and further in view of Takao 5,977,594. Ker discloses (see, for example, column 6, lines 38-41) a gate structure 132 comprising a gate oxide layer. Ker does not disclose a protective film and a conductive material formed on the protective film. However, Takao discloses (see, for example, FIG. 1B) a protecting circuit comprising an oxide film

(protective film) OXIDE FILM and metal wire (conductive material) M1, M2, M3, M4. The oxide film protects the semiconductor device and the metal wire provides connections to the diffused regions. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have a protective film and a conductive material formed on the protective film in order to protect the device and have connections to the diffused regions.

13. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. '566 B2 in view of Takao '594 as applied to claim 2 above, and further in view of Harari 4,072,976. Ker in view of Takao does not disclose the gate of the field effect transistor being comprised of metal. However, Harari discloses (see, for example, column 5, lines 26-46) a gate protection device comprising a gate electrode made of metal. The gate electrode has low resistance and provides a reliable connection to the substrate. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have the gate of the field effect transistor being comprised of metal in order to have a low resistance and provide a reliable connection to the substrate.

14. Insofar as definite, claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. '566 B2 as applied to claims 1 and 6 above, and further in view of Hirata 6,469,354 B1. Ker does not disclose a plurality of field effect transistors which are provided in the well region; and wherein the field effect transistors share a gate and drain. However, Hirata discloses (see, for example, FIG. 4B) a protective circuit comprising field effect transistors 33, 34 in a P-well 11a and wherein the field effect transistors share gates electrodes 15n and diffused regions

(drain). In column 6, lines 62-64, Hirata discloses the protective circuit prevents ESD surge from being transmitted to an internal circuit to thereby protect the internal circuit. Therefore it would have been obvious to one of ordinary skill in the art at the time of invention to have a plurality of field effect transistors which are provided in the well region; and wherein the field effect transistors share a gate and drain in order to prevent ESD surge and protect the internal circuit.

15. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. '566 B2 as applied to claims 1 and 6 above, and further in view of Hayashida et al. 6,760,204 B2 in view of Yamada et al. 5,748,459 in view of Sakamoto et al. 5,638,246. Ker does not disclose an impedance element. However, Hayashida discloses (see, for example, FIG. 3) a semiconductor integrated circuit device comprising an input resistance (impedance element) Rin in between electrostatic protective device 11a and CDM protective device 13a. In column 10, lines 65-column 11, line 2, Hayashida discloses the protective devices may be a MOSFET (field effect transistor) or diode. It would have been obvious to one of ordinary skill in the art at the time of invention to have an impedance element in order to drive a signal into a semiconductor device.

Ker in view of Hayashida does not disclose the impedance element having larger impedance than the impedance of the field effect transistor. However, Yamada discloses (see, for example, column 22, lines 45-47) a resistor wherein the resistor has a greater value than that of a transistor. Yamada further discloses the resistor of greater value is used to drive the transistor. Therefore it would have been obvious to one of ordinary skill in the art at the time of

invention to have the impedance element having larger impedance than the impedance of the field effect transistor and a diode in order to drive a semiconductor component.

Ker in view of Hayashida in view of Yamada does not disclose the impedance element having larger impedance than the impedance of the diode. However, Sakamoto discloses (see, for example, column 4, lines 25-34) a protection circuit comprising diodes and a resistor having a resistance incomparably greater than the impedance of the diodes. It would have been obvious to one of ordinary skill in the art at the time of invention to have the impedance element having larger impedance than the impedance of the diode in order to protect the internal circuit with the resistor.

16. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ker et al. 6,573,566 B2 in view of Matsumoto 6,462,383 B1. Ker discloses (see, for example, FIG. 9C) a semiconductor device comprising an internal circuit and a protection circuit comprising an SOI-SCR 314 wherein the SOI-SCR comprises a PN junction (first element) and a field effect transistor (second element). Ker does not disclose the internal circuit, connected to a plurality of terminals. However, Matsumoto discloses (see, for example, FIG. 7A) an input circuit (internal circuit) connected to a protection element in between a plurality of terminals. It would have been obvious to one of ordinary skill in the art at the time of invention to have the internal circuit, connected to a plurality of terminals, in order to properly connect the internal circuit to the protection circuit so that the internal circuit is protected from voltage surges or static charges.

Regarding the limitation "having a rising edge of current equivalent to that of a diode as a response to current that flows according to potential difference between the terminals; and a

second element, having, having a impedance equivalent to that of a transistor after the rise edge of current", Ker in view of Matsumoto has the same structure and materials as the claimed invention, and inherently have the same electrical characteristics.

INFORMATION ON HOW TO CONTACT THE USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eugene Lee whose telephone number is 571-272-1733. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eugene Lee
September 3, 2004